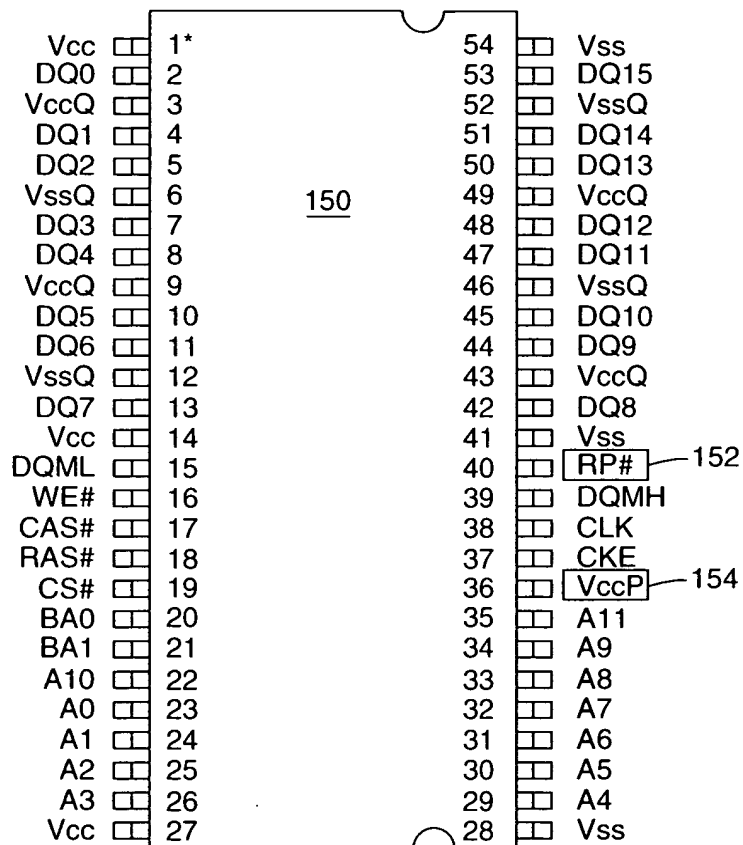


Fig. 1A

*Fig. 1B*

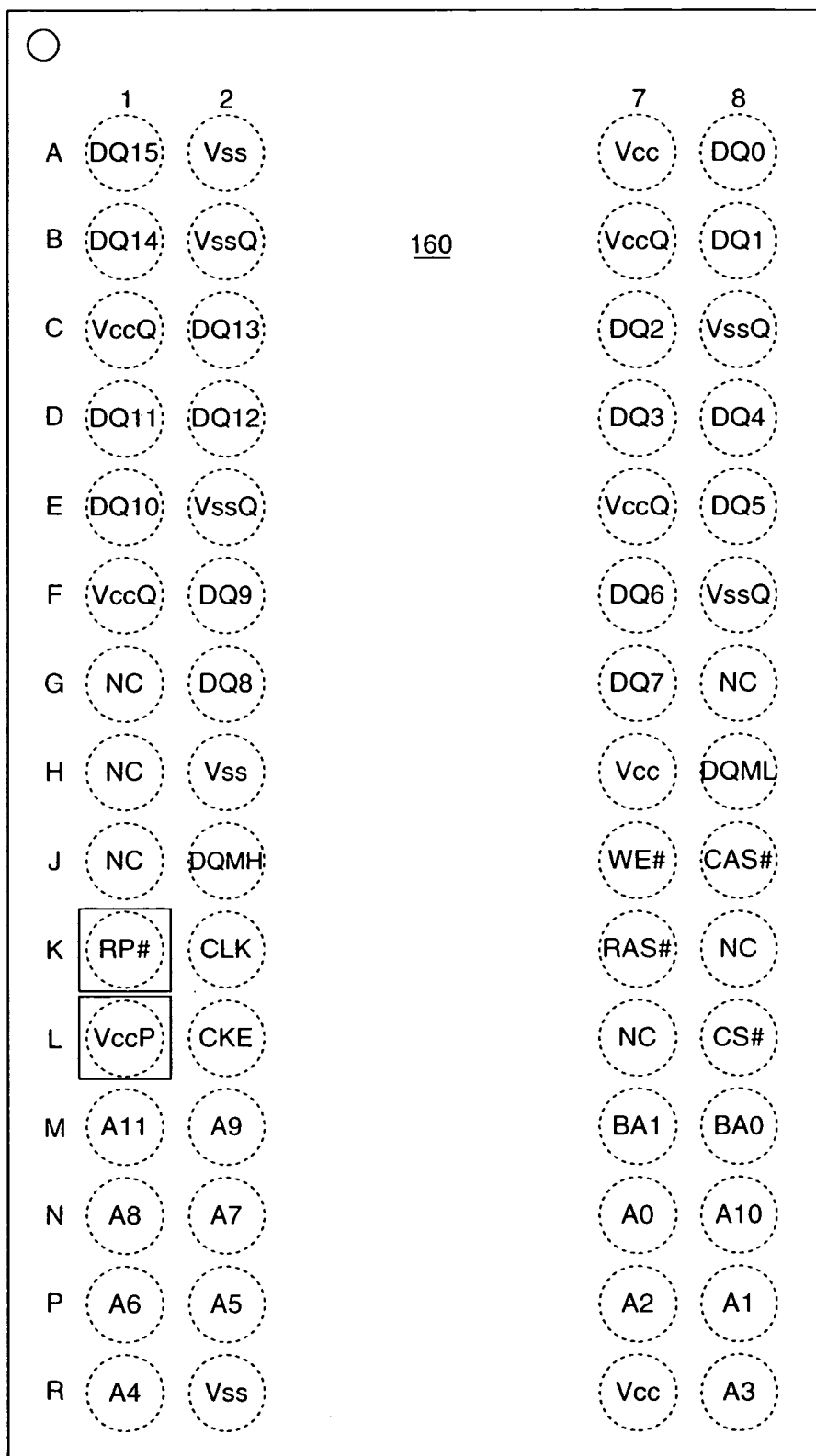


Fig. 1C

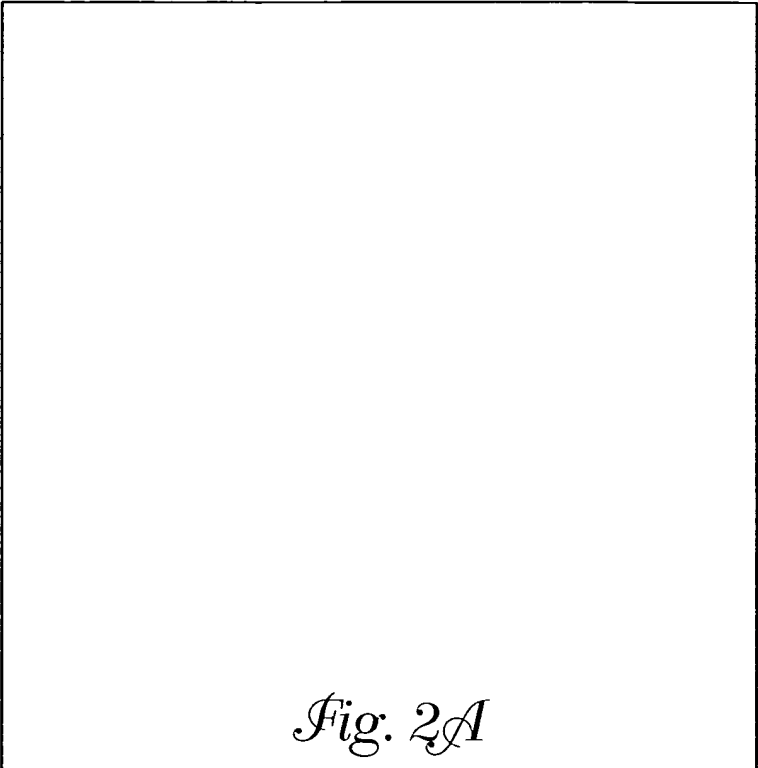


Fig. 2A

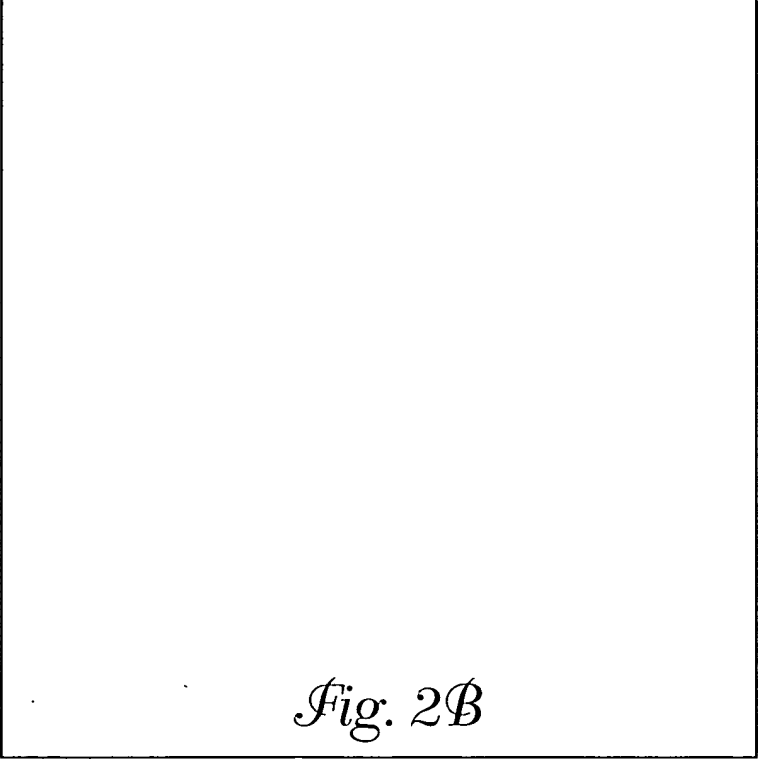
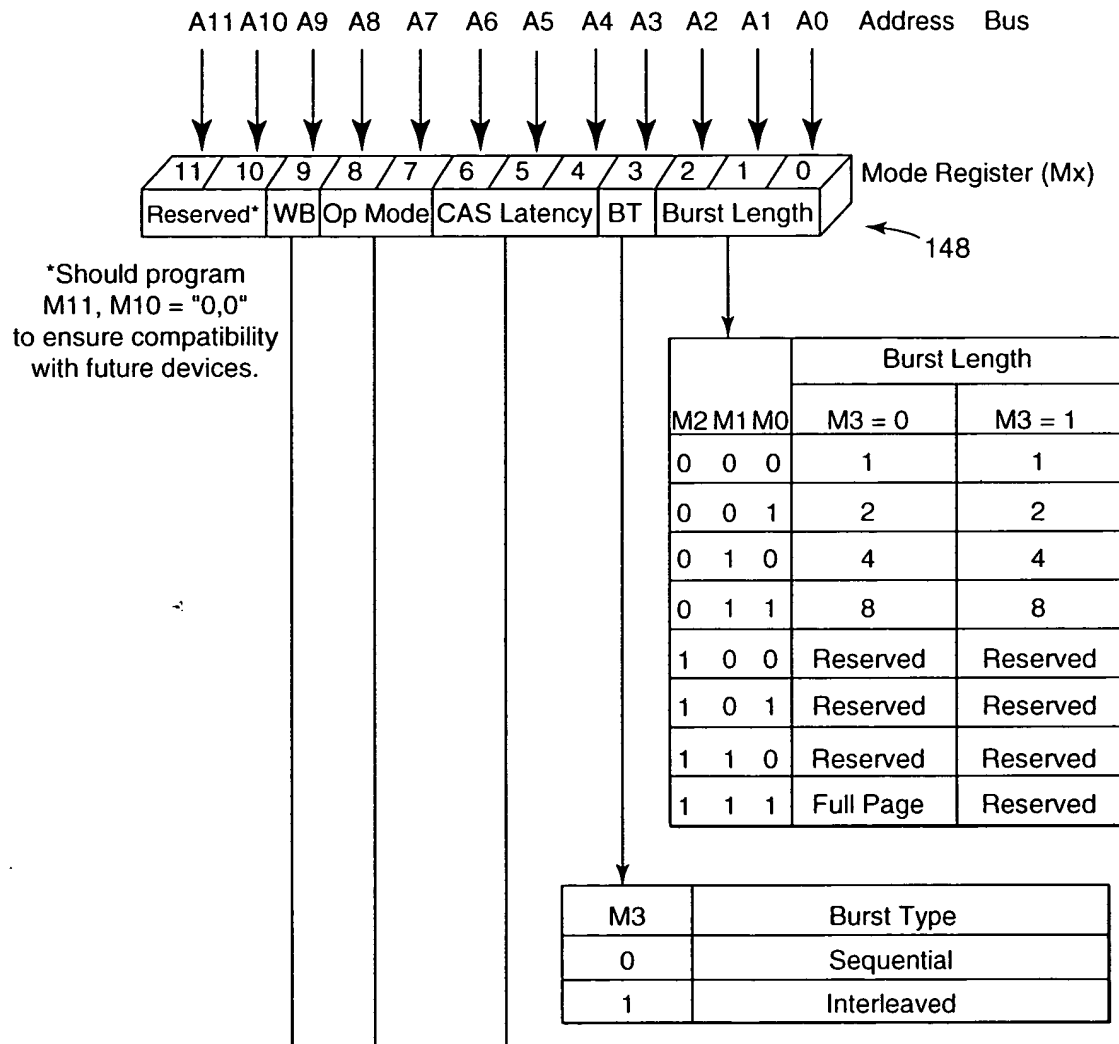
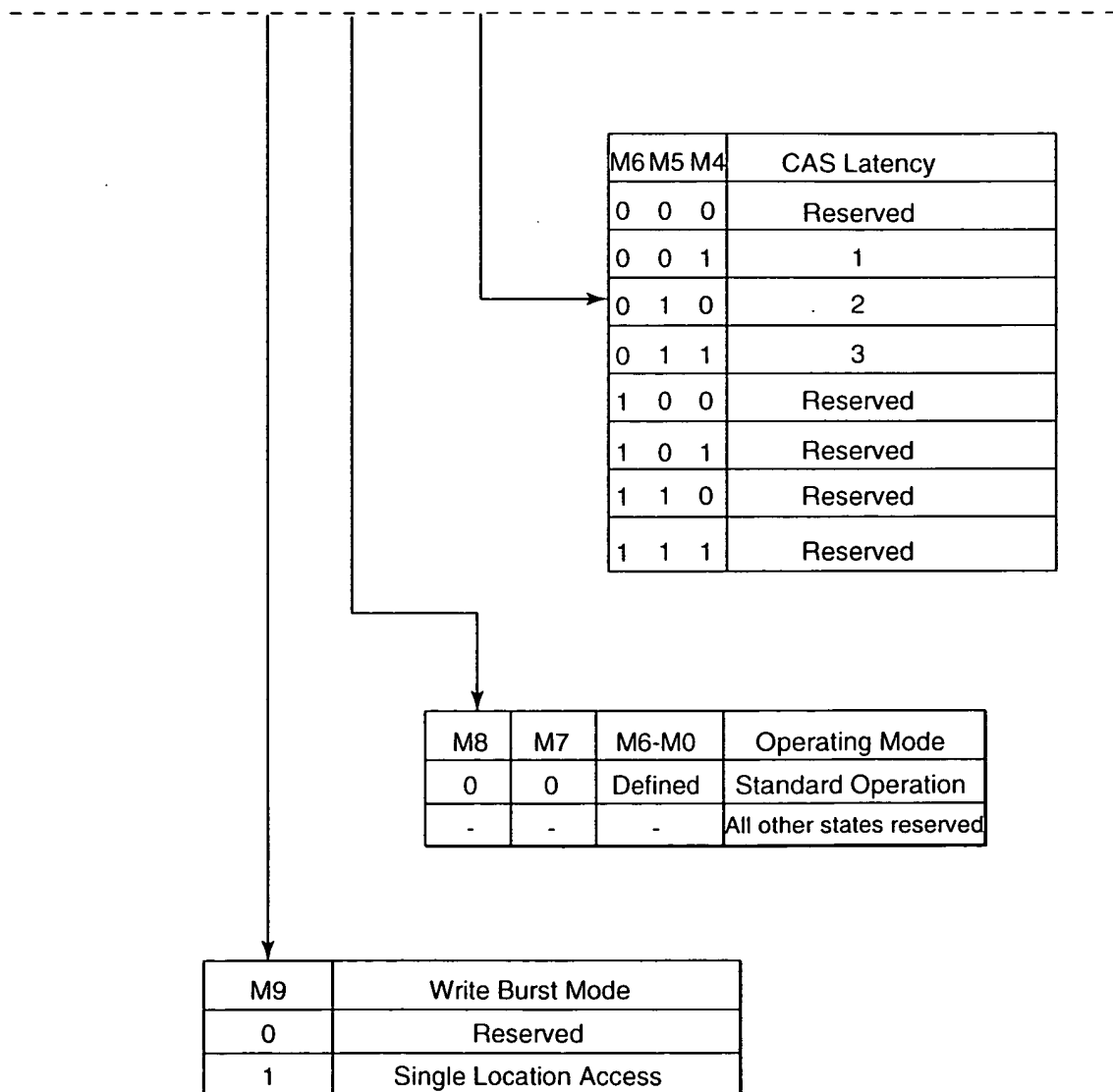


Fig. 2B

Fig. 2

*Fig. 2A*

*Fig. 2B*

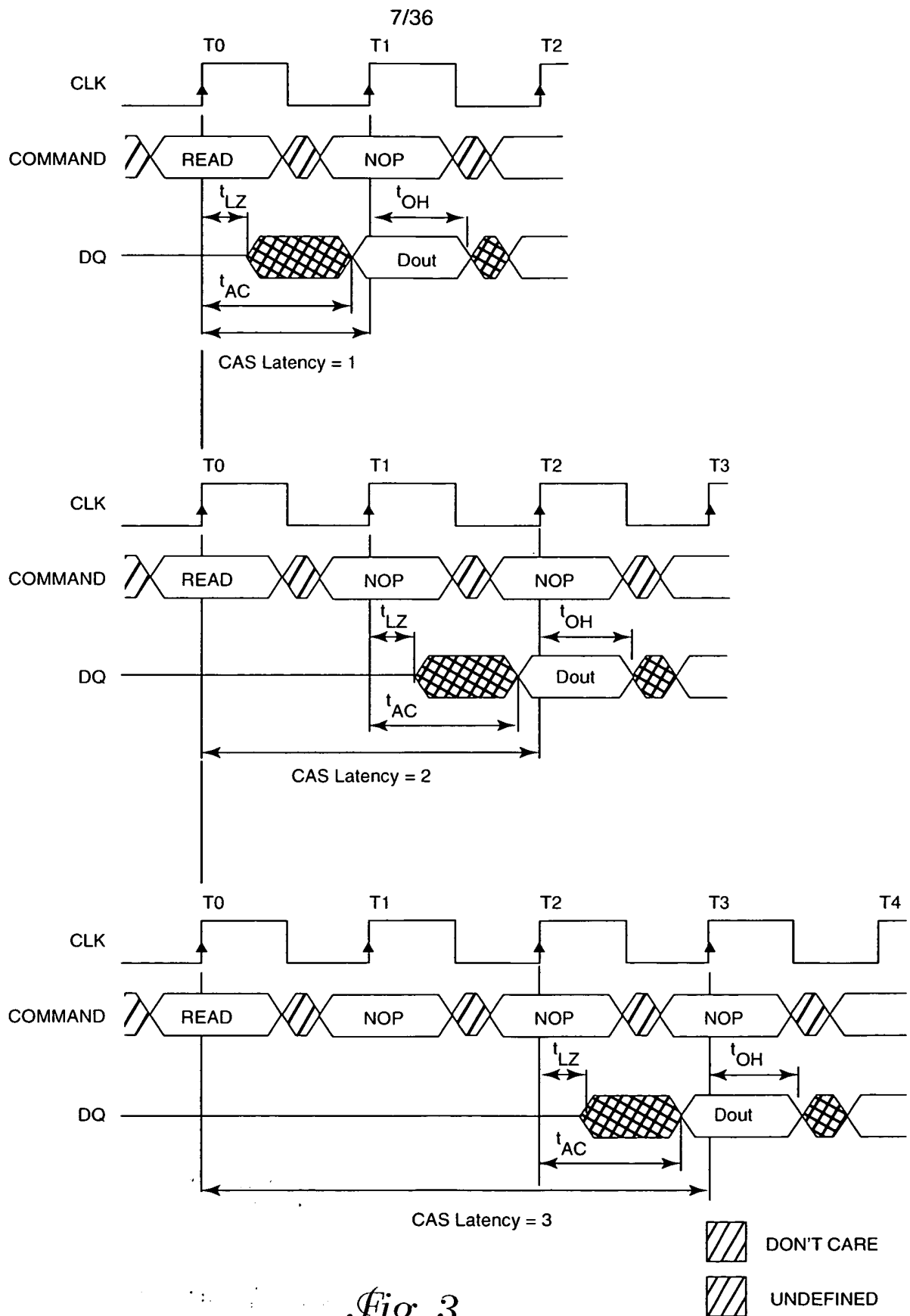


Fig. 3

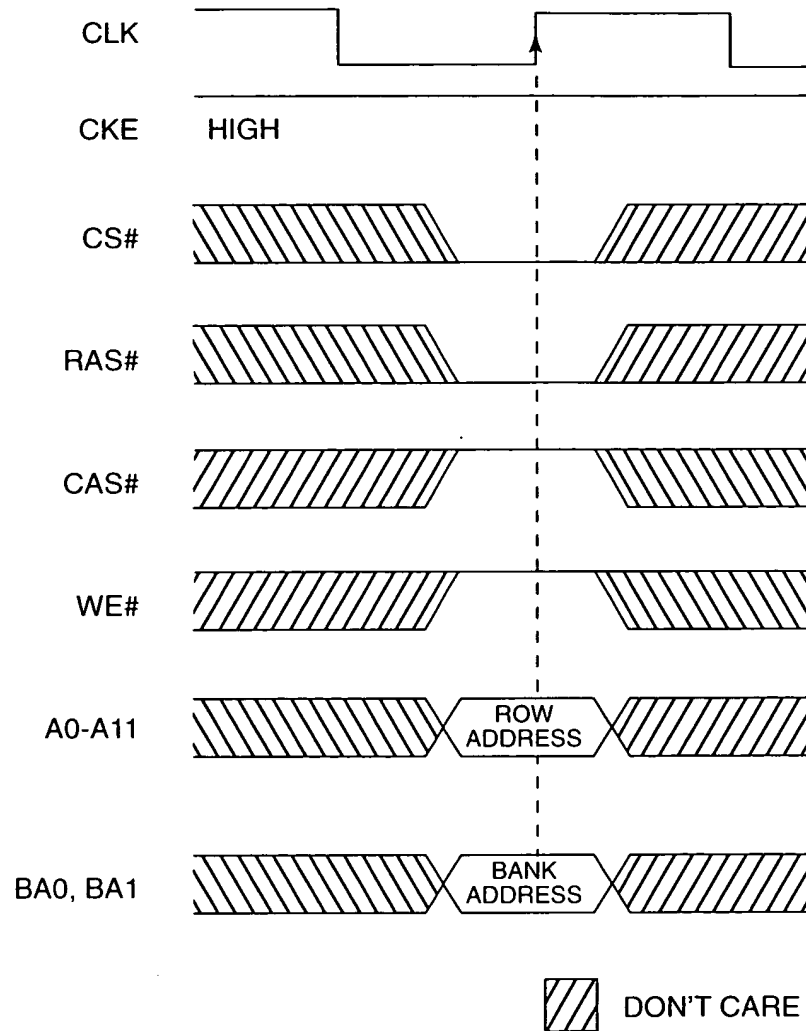


Fig. 4

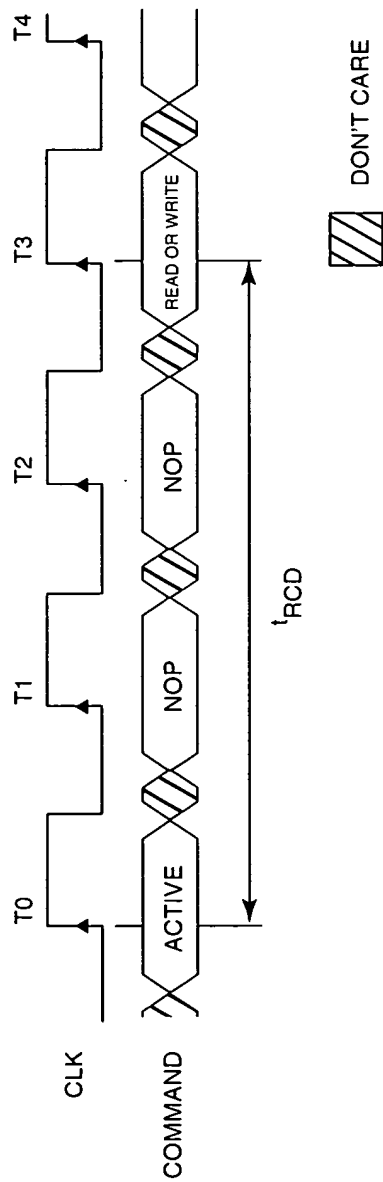


Fig. 5



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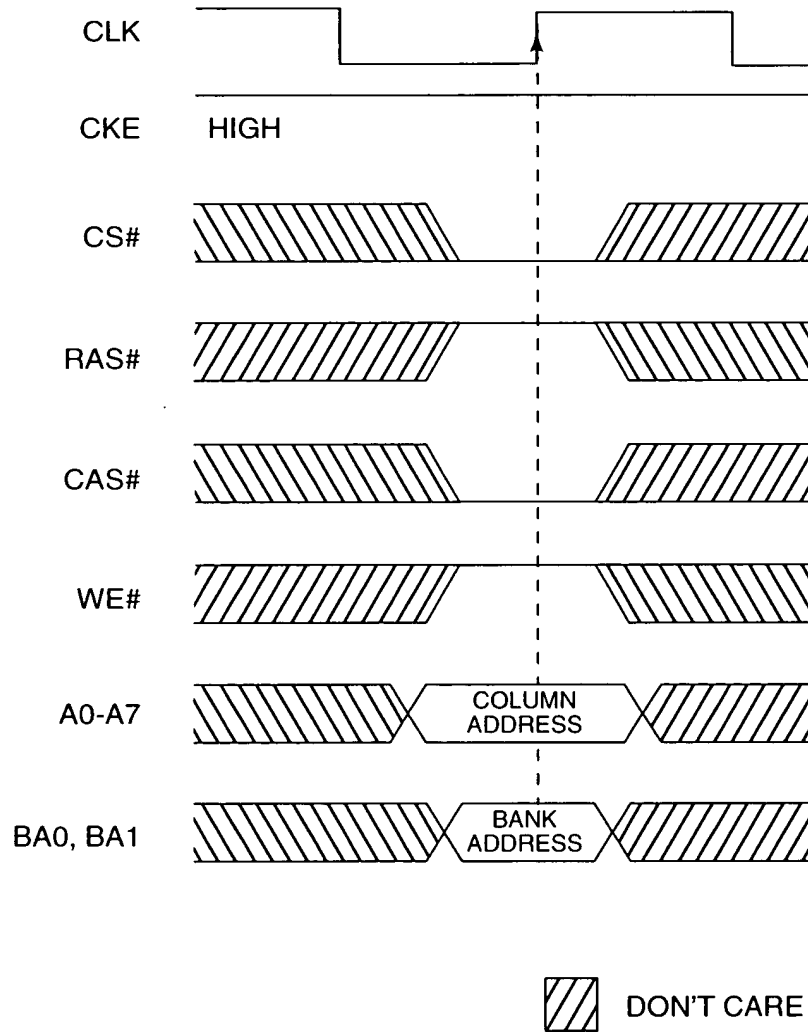
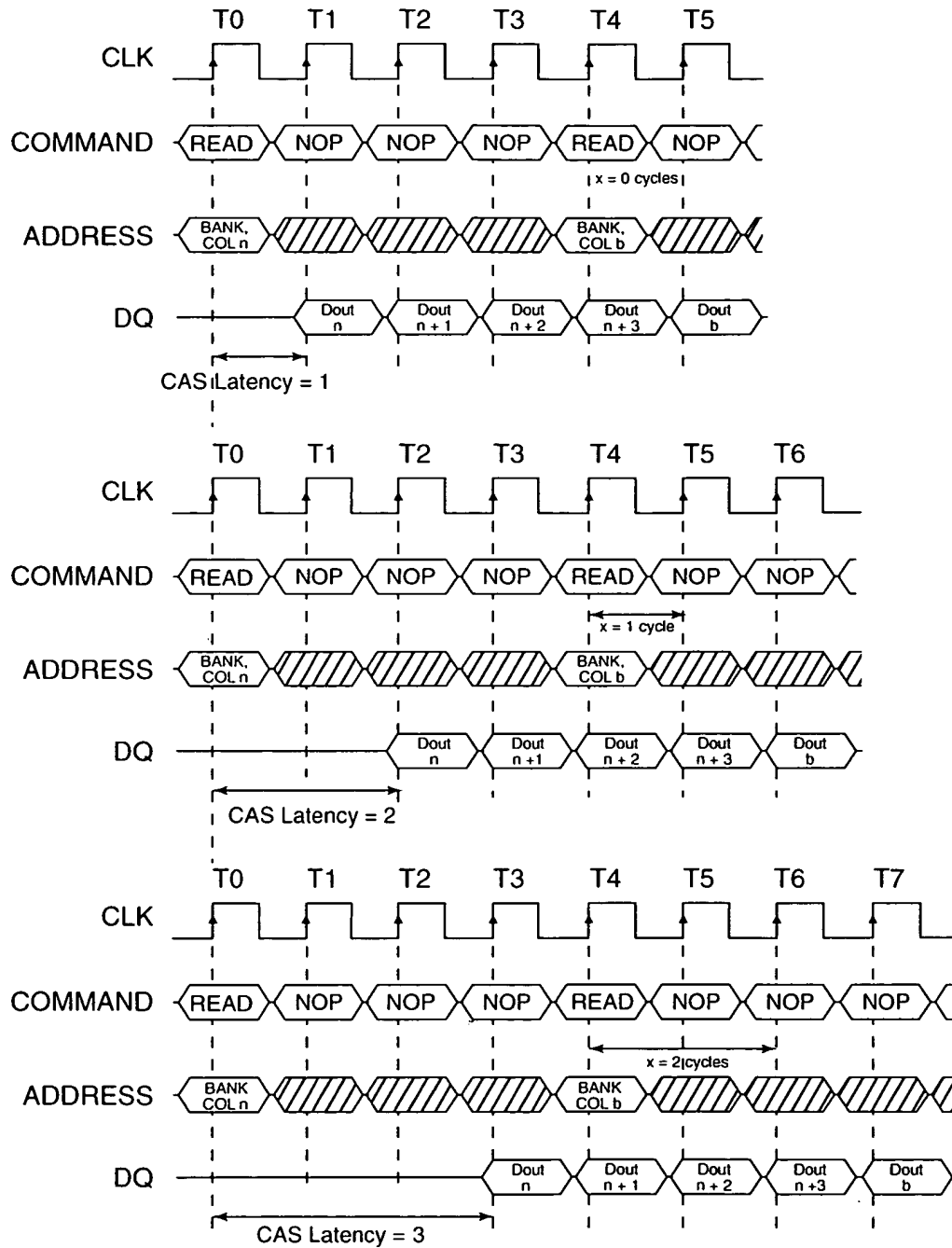


Fig. 6



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 DON'T CARE

NOTE: Each READ command may be to either bank. DQM is LOW.

Fig. 7

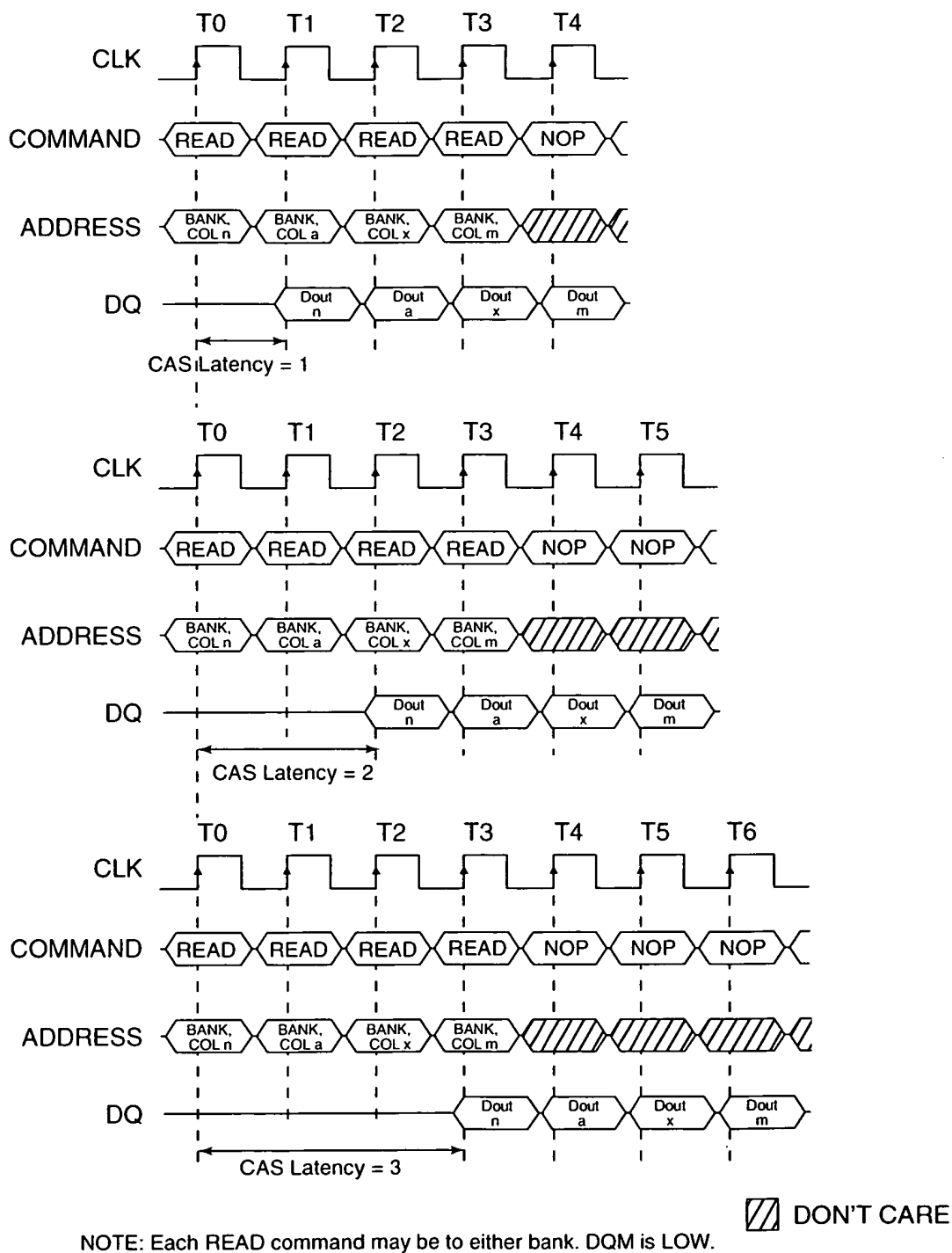
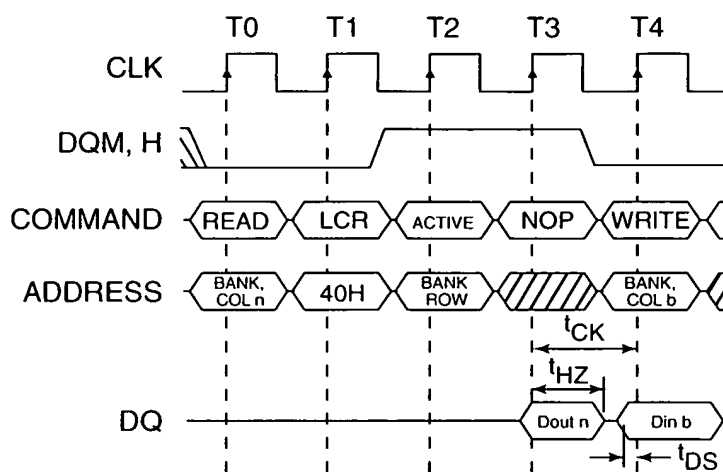


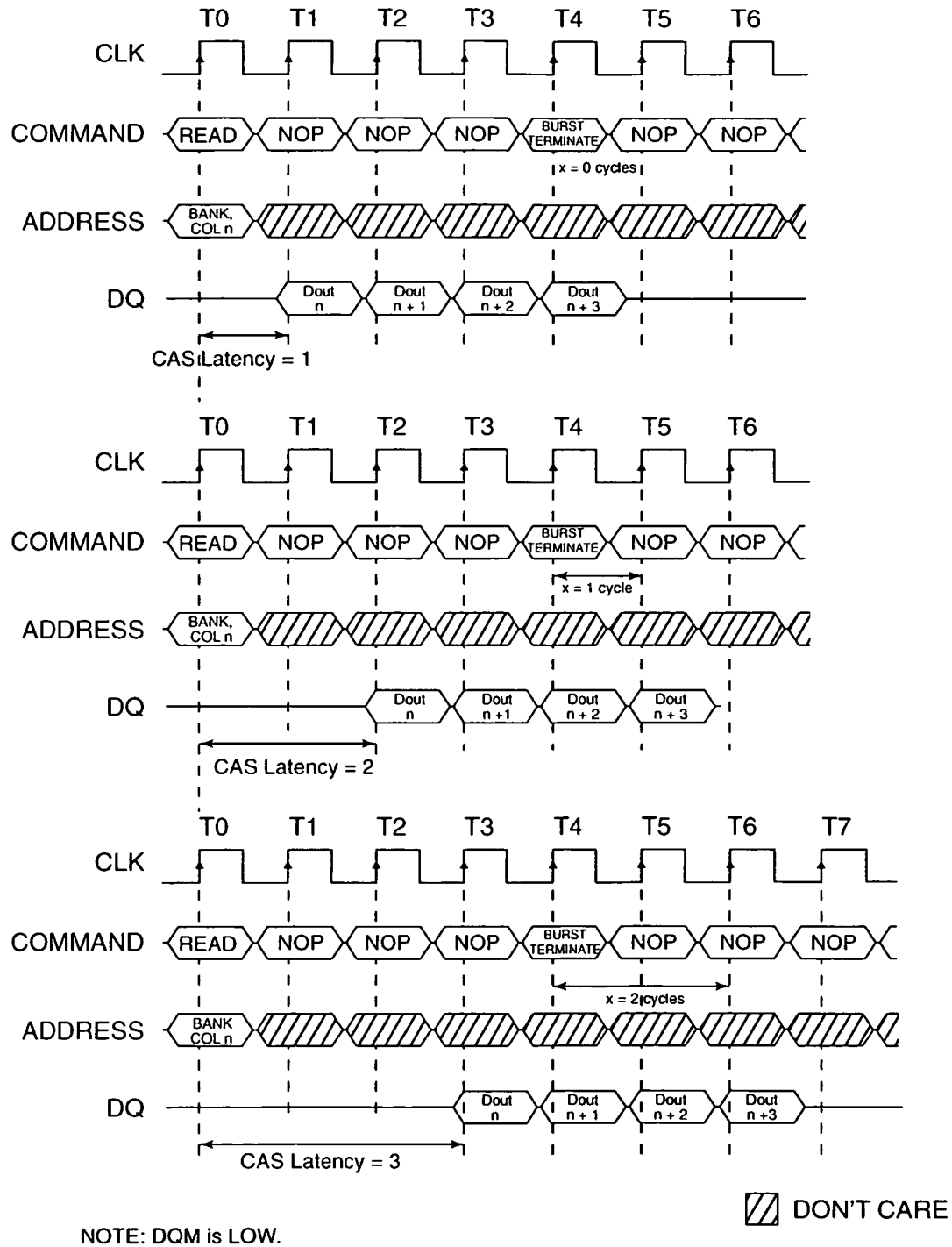
Fig. 8

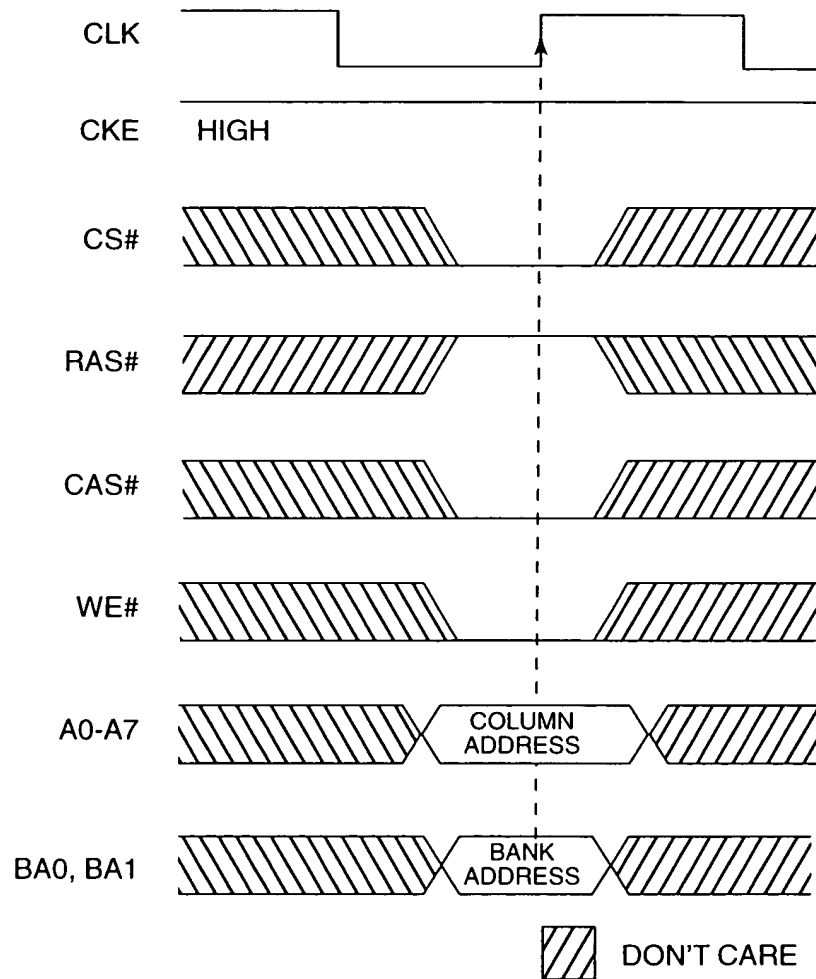


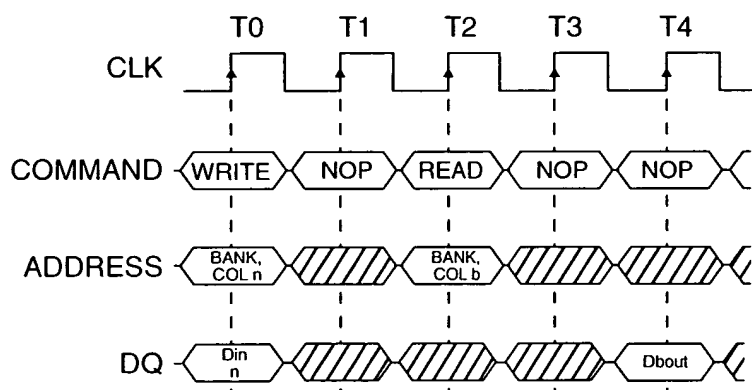
NOTE: A CAS latency of three is used for illustration. The READ command may be to any bank, and the WRITE command may be to any bank. If a CAS latency of one is used, then DQM is not required.

 DON'T CARE

Fig. 9

*Fig. 10*

*Fig. 11*



NOTE: A CAS latency of two is used for illustration. The WRITE command may be to any bank and the READ command may be to any bank. DQM is LOW. A READ to the bank undergoing the WRITE ISM operation may output invalid data. For more details, refer to Truth Tables 4 and 5.

 DON'T CARE

Fig. 12

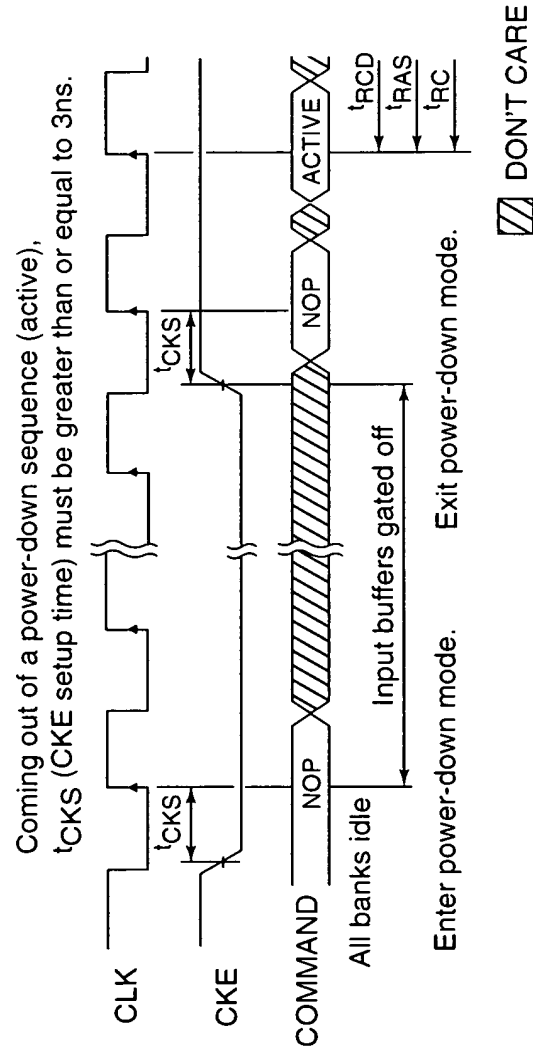


Fig. 13

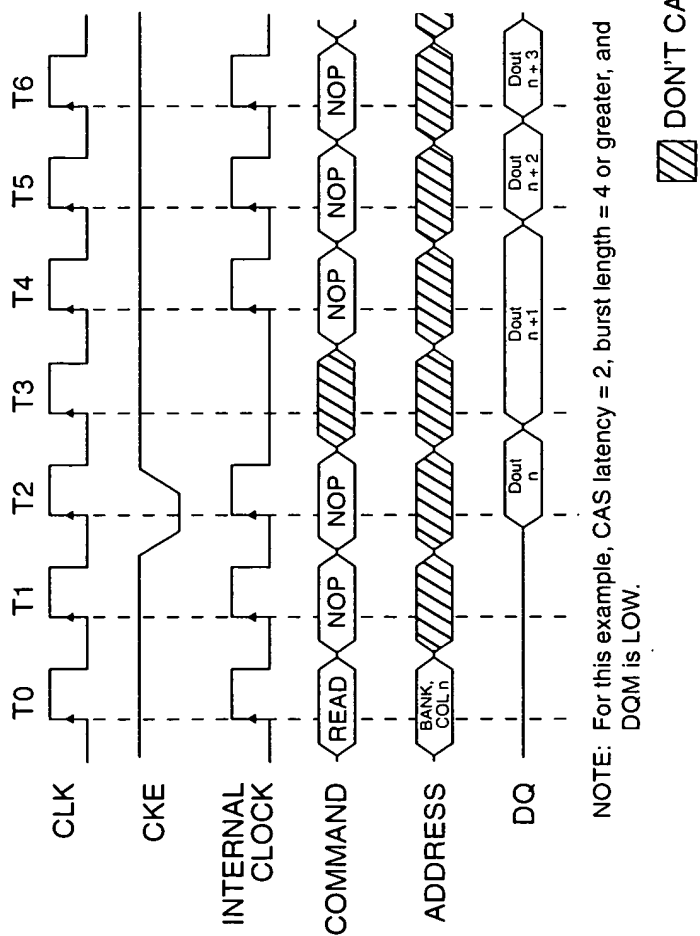



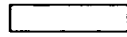
Fig. 14



ADDRESS RANGE

	Bank	Row	Column		
Bank 3	3	FFF	FFH	256K-Word Block 15	210
	3	C00	00H		
	3	BFF	FFH	256K-Word Block 14	
	3	800	00H		
	3	7FF	FFH	256K-Word Block 13	
	3	400	00H		
	3	3FF	FFH	256K-Word Block 12	
	3	000	00H		
Bank 2	2	FFF	FFH	256K-Word Block 11	
	2	C00	00H		
	2	BFF	FFH	256K-Word Block 10	
	2	800	00H		
	2	7FF	FFH	256K-Word Block 9	
	2	400	00H		
	2	3FF	FFH	256K-Word Block 8	
	2	000	00H		
Bank 1	1	FFF	FFH	256K-Word Block 7	
	1	C00	00H		
	1	BFF	FFH	256K-Word Block 6	
	1	800	00H		
	1	7FF	FFH	256K-Word Block 5	
	1	400	00H		
	1	3FF	FFH	256K-Word Block 4	
	1	000	00H		
Bank 0	0	FFF	FFH	256K-Word Block 3	220
	0	C00	00H		
	0	BFF	FFH	256K-Word Block 2	
	0	800	00H		
	0	7FF	FFH	256K-Word Block 1	
	0	400	00H		
	0	3FF	FFH	256K-Word Block 0	
	0	000	00H		

Word-wide (x16)

-  Software Lock = Hardware-Lock Sectors
RP# = V_{HH} to unprotect if either the
block protect or device protect bit is set.
-  Software Lock = Hardware-Lock Sectors
RP# = V_{CC} to unprotect but must be V_{HH}
if the device protect bit is set.

See BLOCK PROTECT/UNPROTECT SEQUENCE for
detailed information.

Fig. 15



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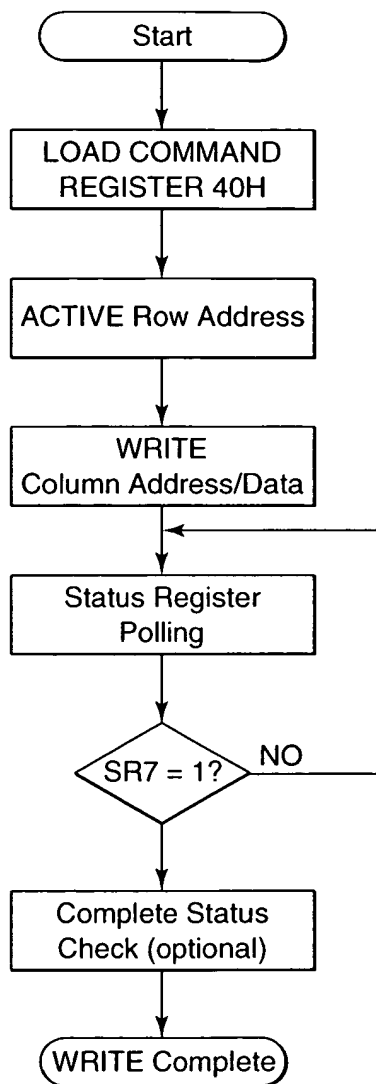


Fig. 16

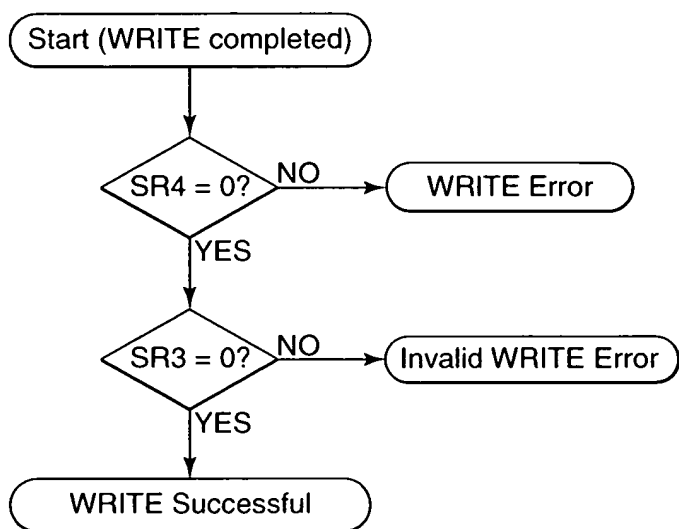
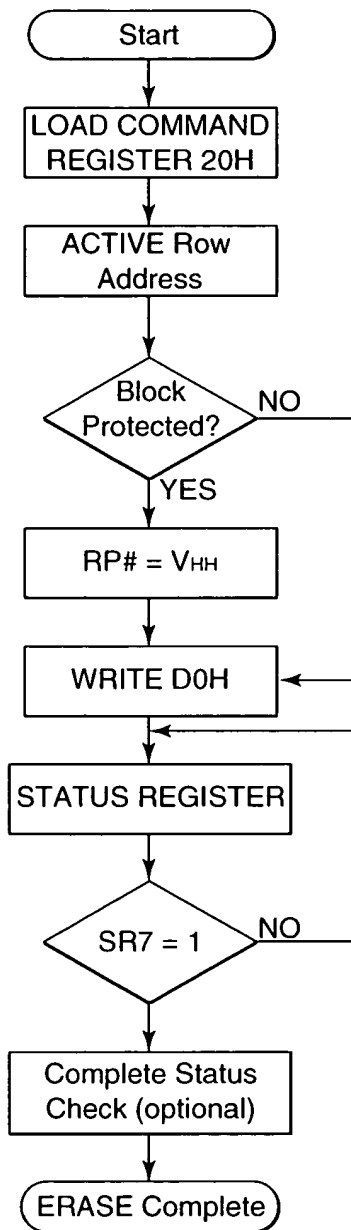
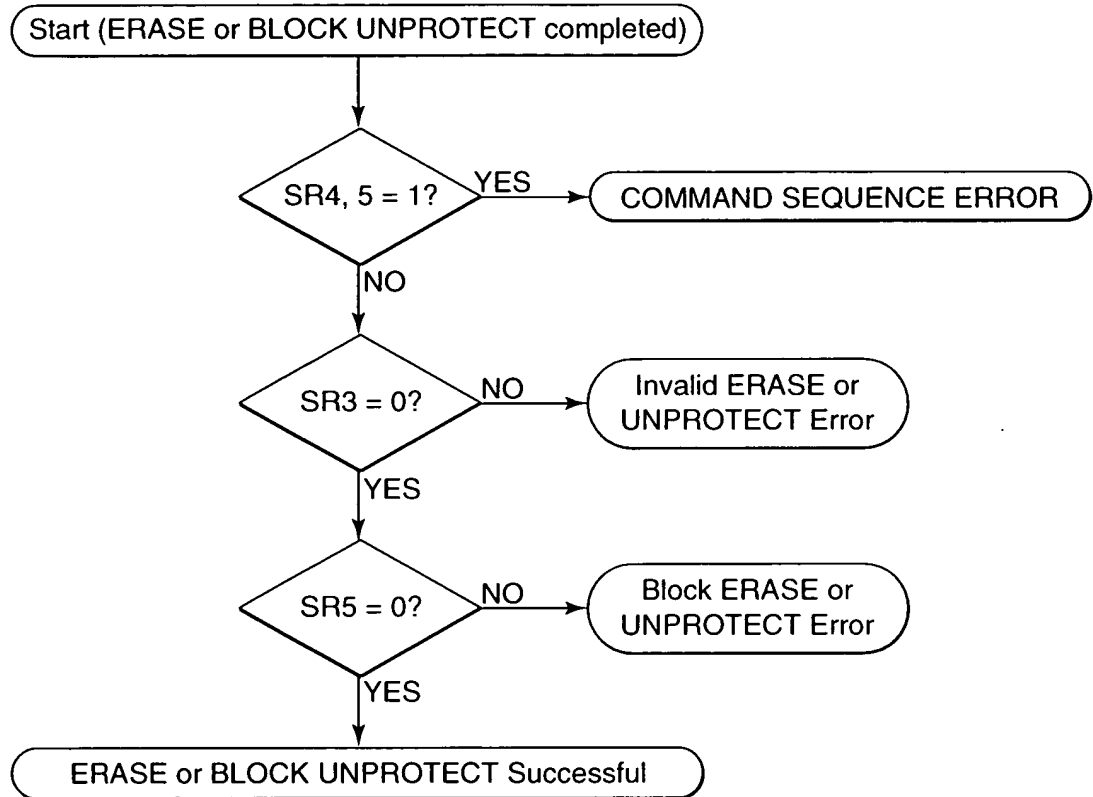
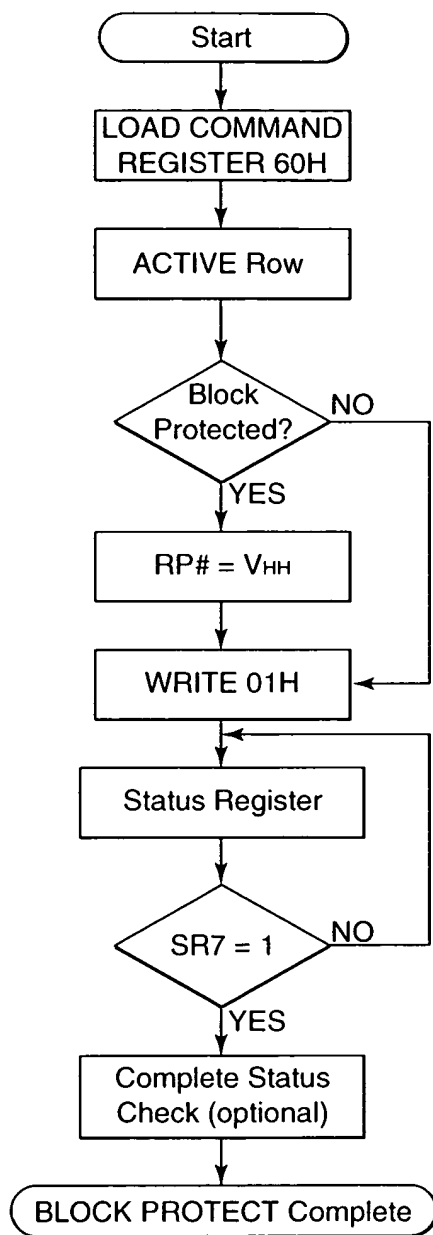
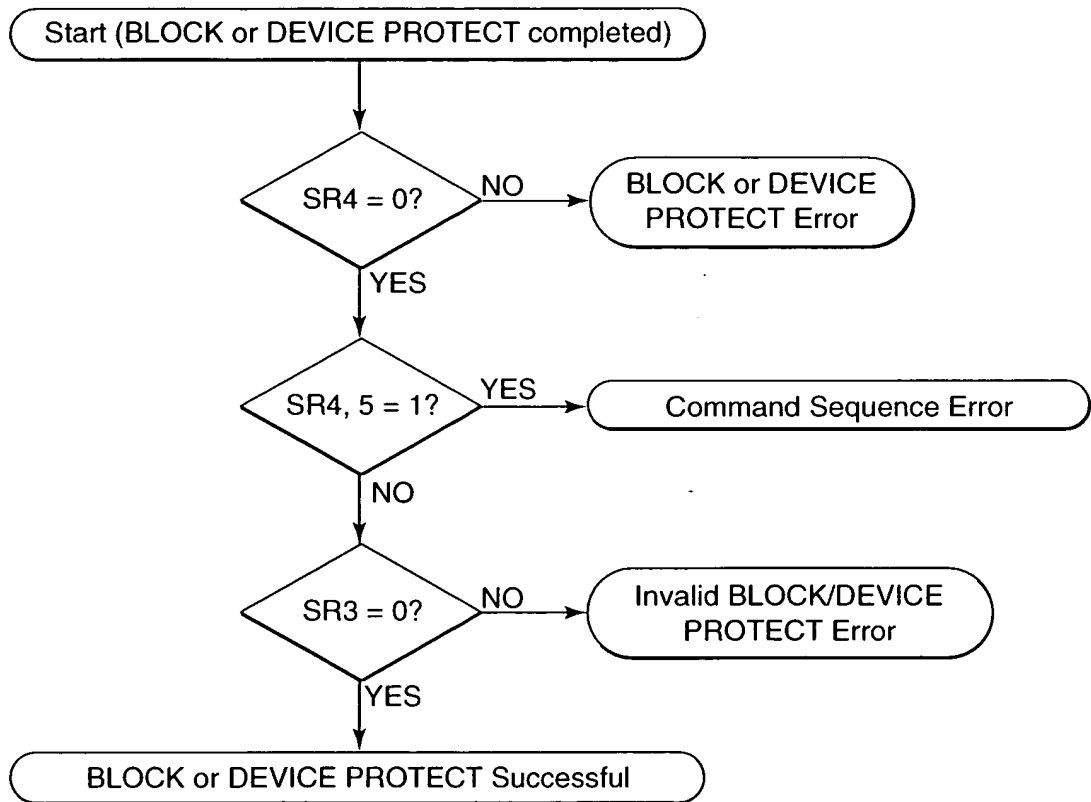


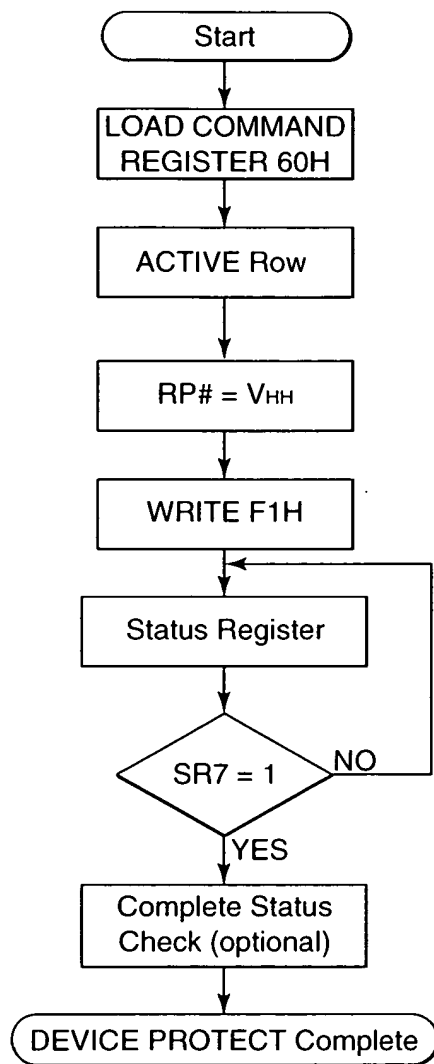
Fig. 17

*Fig. 18*

*Fig. 19*

*Fig. 20*

*Fig. 21*

*Fig. 22*



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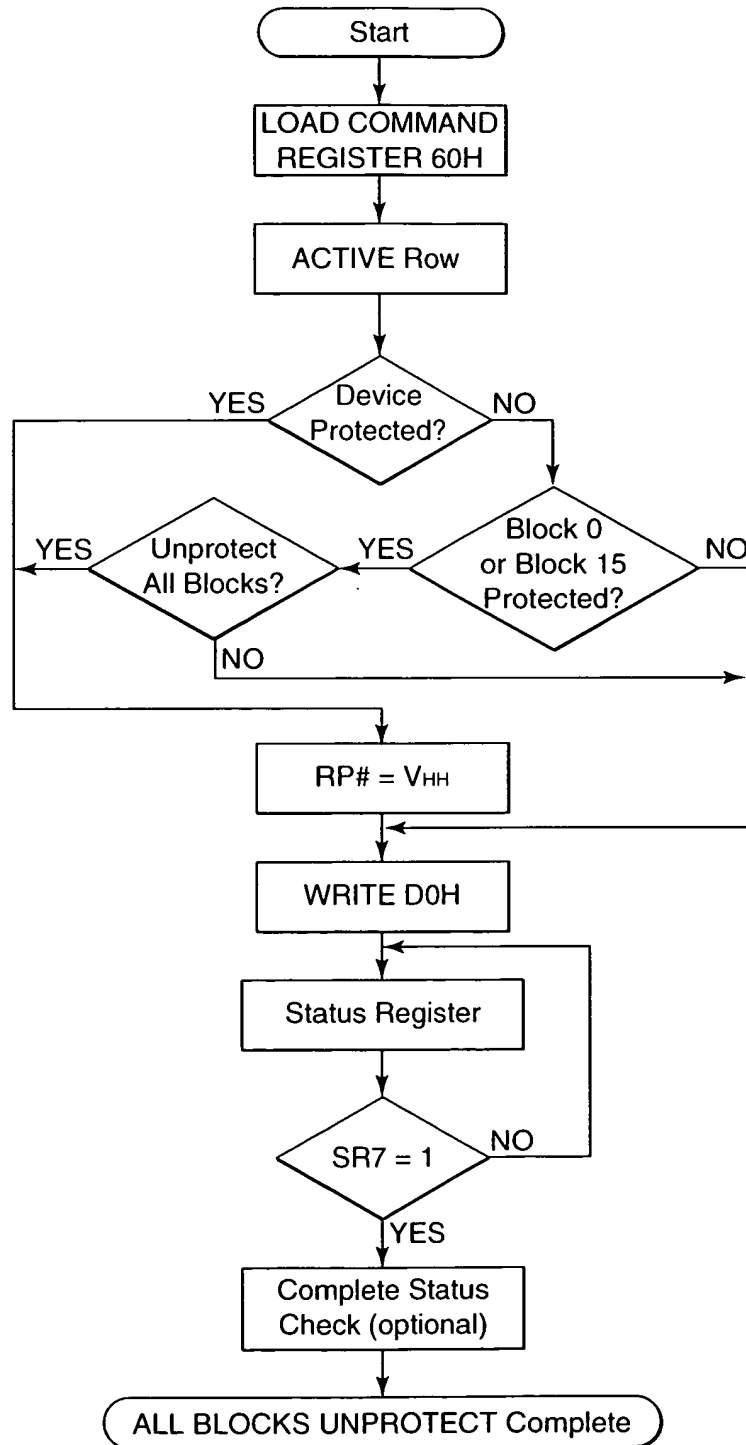
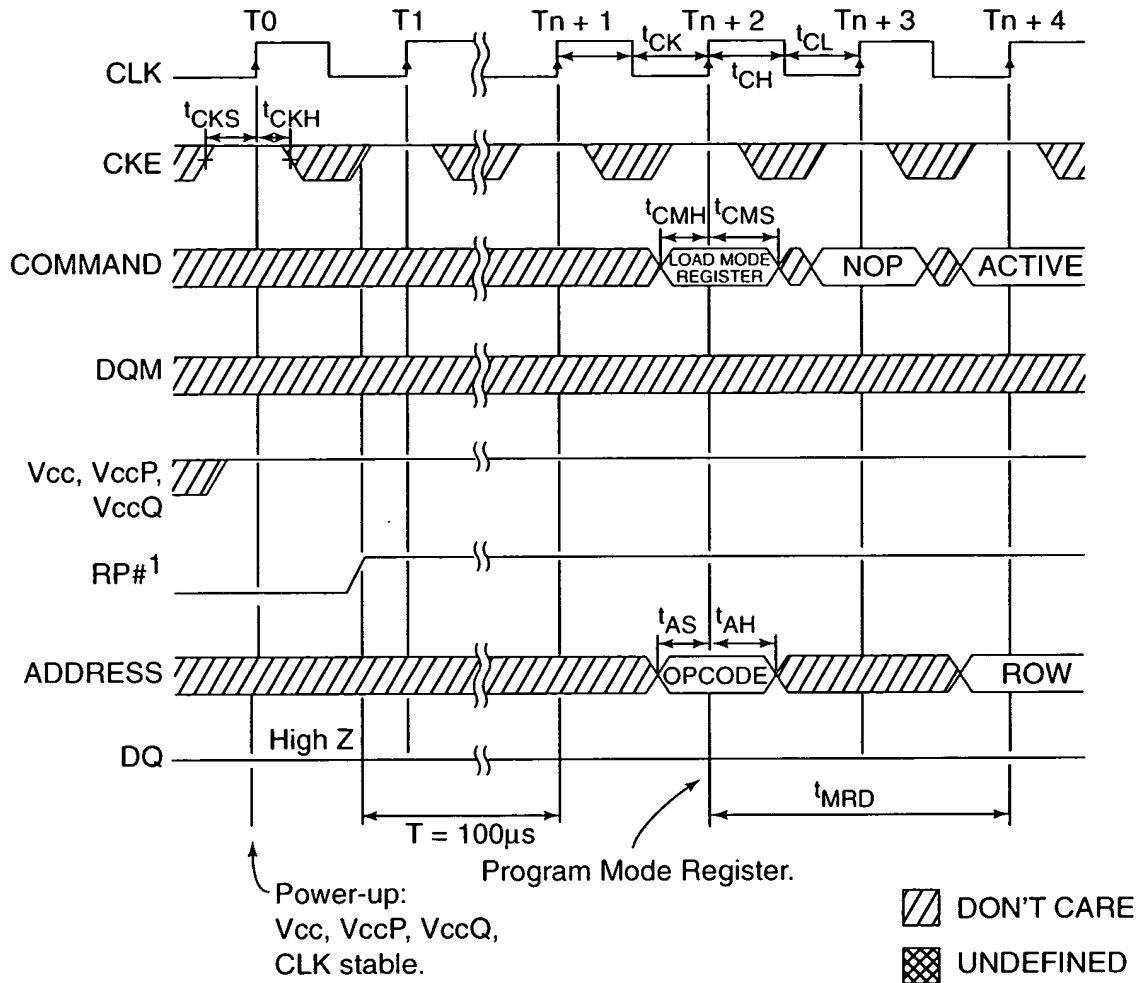


Fig. 23

*Fig. 24*

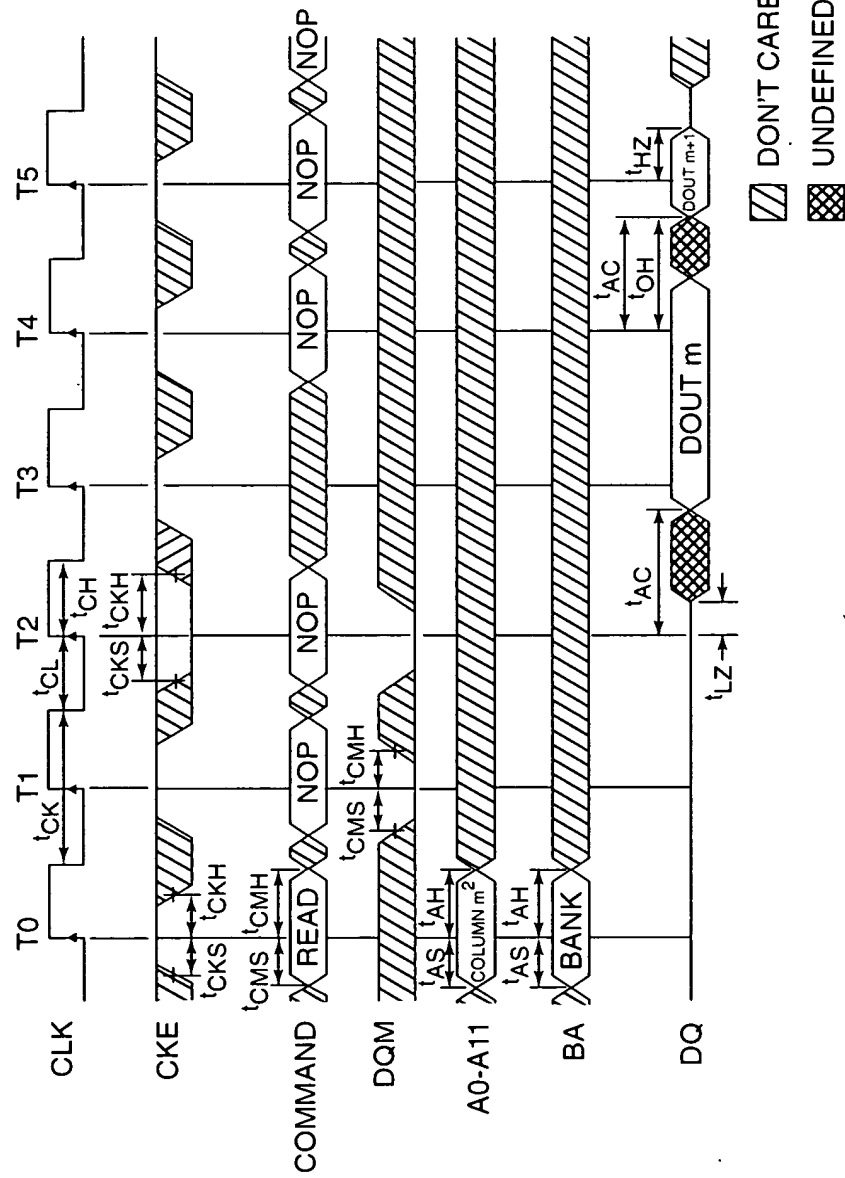


Fig. 25

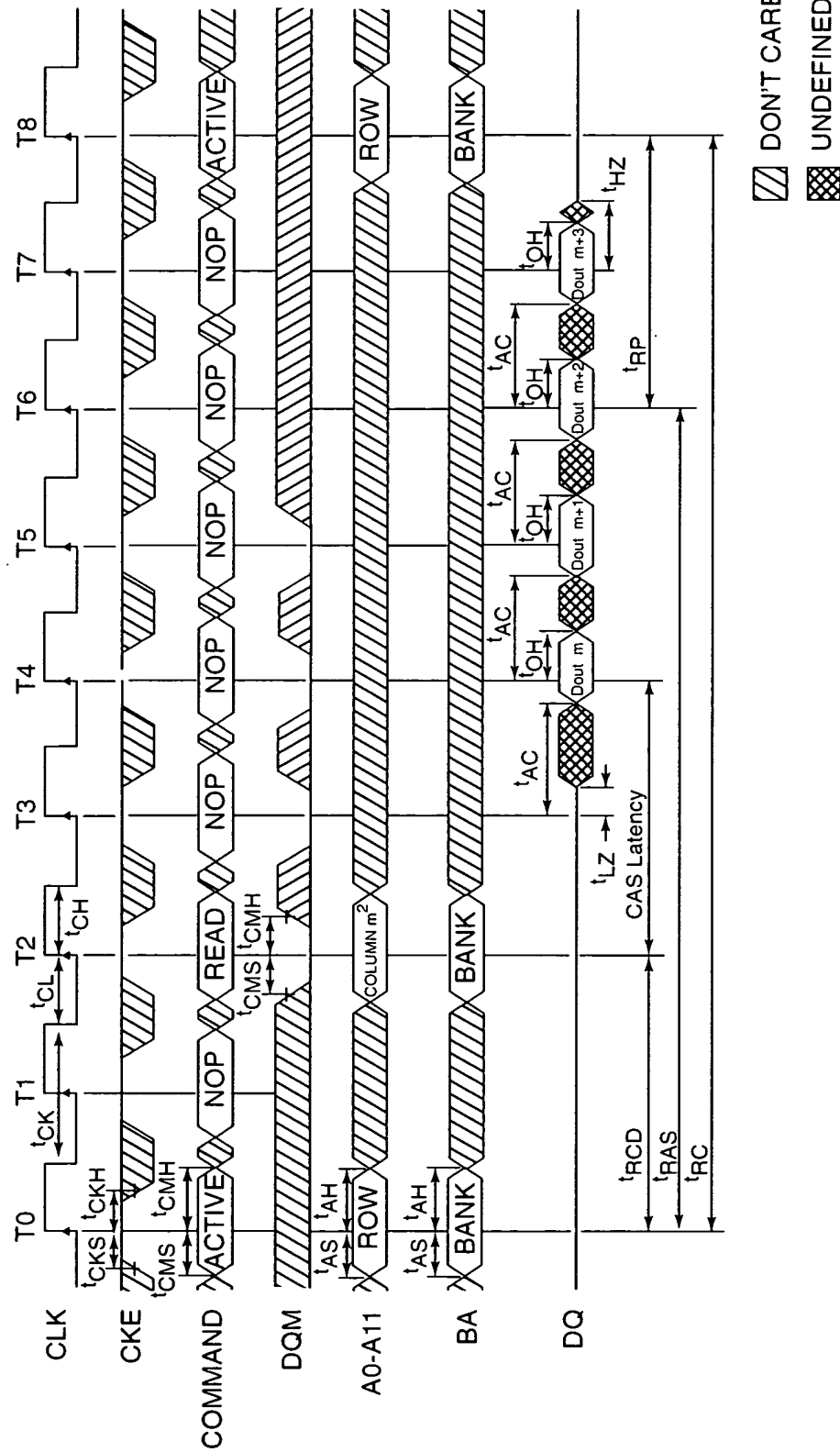
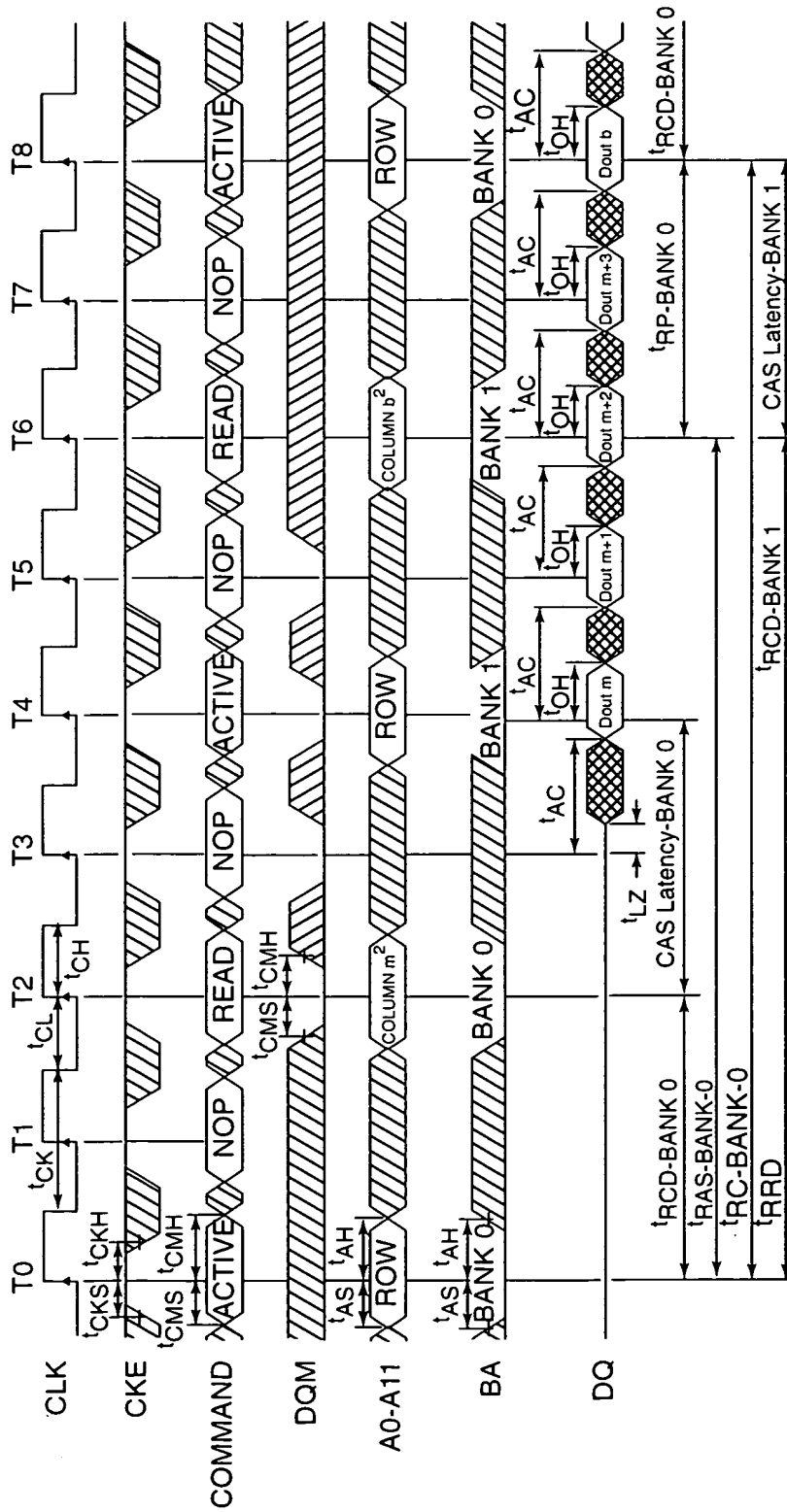


Fig. 26



DON'T CARE
 UNDEFINED

Fig. 27

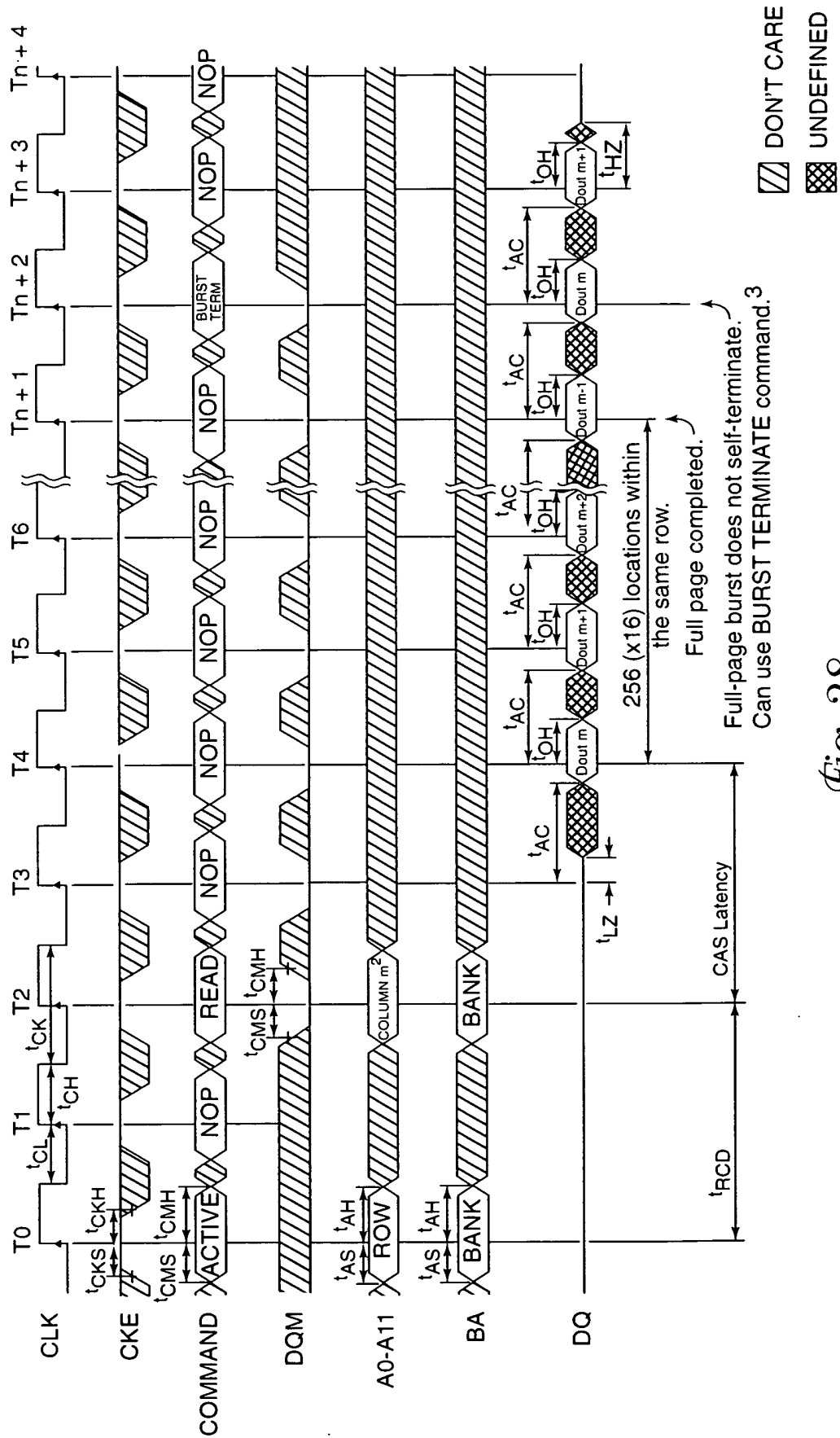


Fig. 28

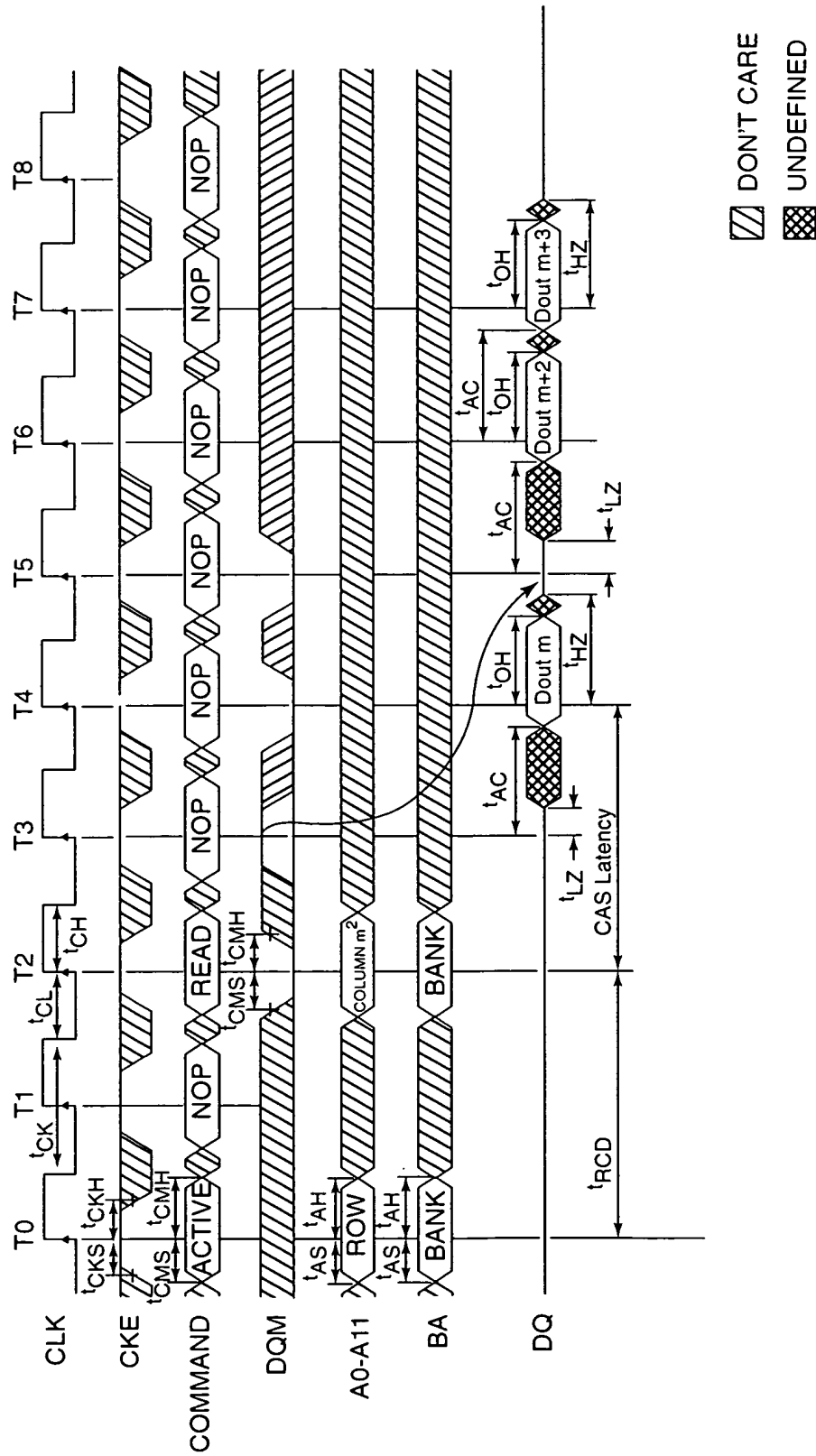


Fig. 29

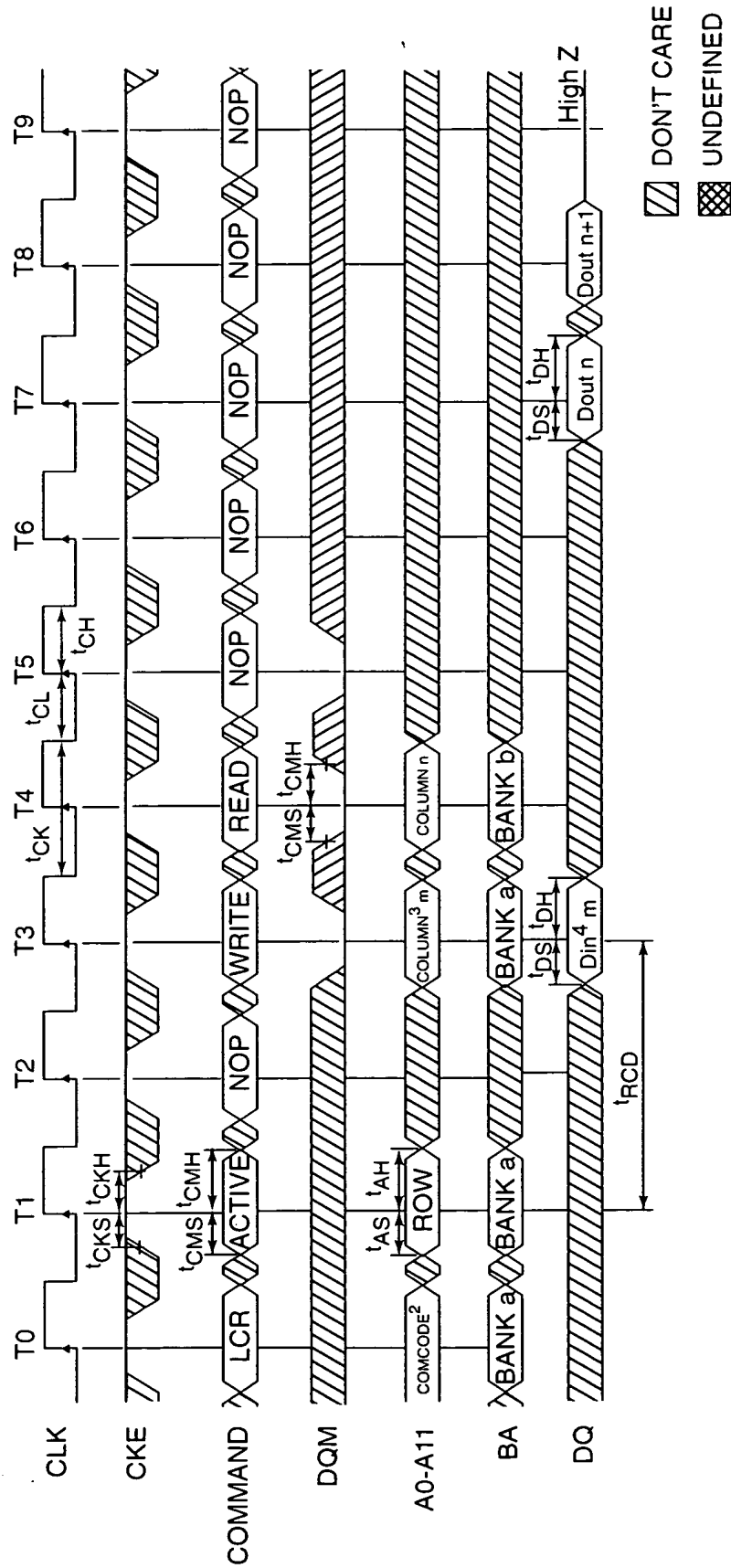


Fig. 30

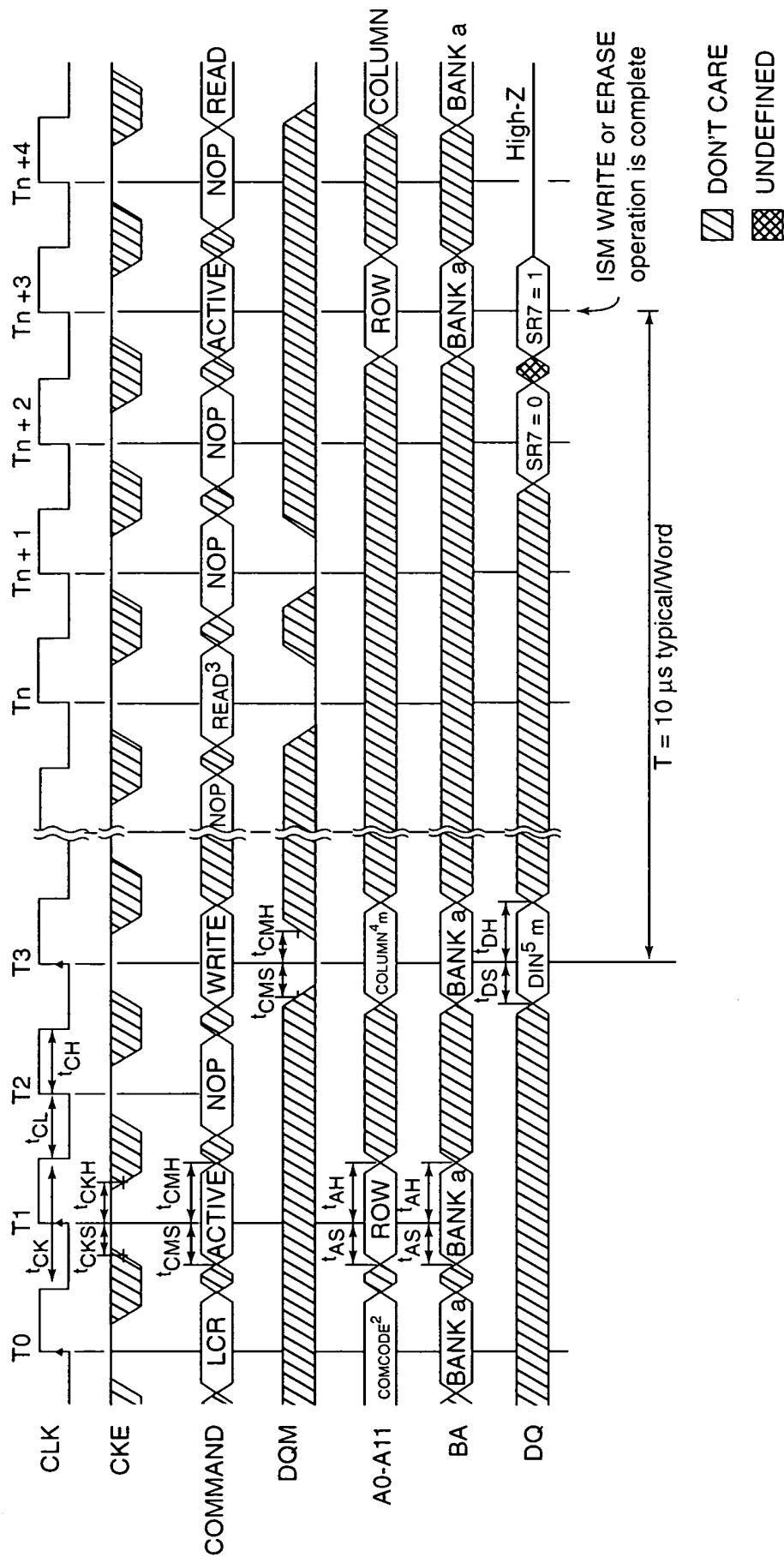


Fig. 31



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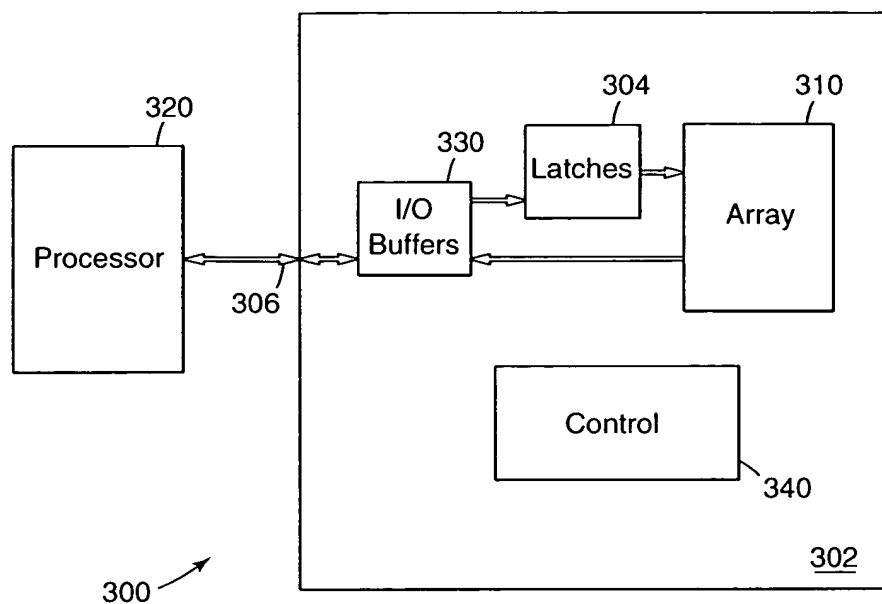


Fig. 32

Fig. 33

